ABSTRACT

A phase locked loop frequency synthesizer with jitter compensation having a tapped delay line for compensating the jitter prior to passing a signal subject to jitter through a non-linearity; and, a ΣΔ modulator for generating, or a storing element for pre-generated storing, of a fractional pattern representing fractional weighting of a plurality of integer divisors, wherein the fractional pattern identifies one integer divisor, out of the plurality of integer divisors, at a time to be active.